The Particle/Photon to Digital Converters

Jean-Francois Pratte[1], Serge A. Charlebois[1], Thomas Brunner[2], Reiner Kruecken[3], Fabrice Retière[3], and Simon Viel[4]

[1]Université de Sherbrooke, QC, Canada
[2]McGill University, QC, Canada
[3]TRIUMF, BC, Canada
[4]Carleton University, ON, Canada

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Silicon Photo-multiplier (SiPMs) have been widely used in particle physics for more than a decade. SiPMs are arrays of single photon avalanche diodes (SPADs) connected together in parallel. They are ideally suited for applications requiring the detection of small light flashes (1-10,000 photons) over short time scales (ps to μs scale). Their dark noise rate (100 kHz/mm^2 at room temperature) can be mitigated by having bright and short light flashes and/or when cooling is possible. Excellent (less than 100 ps) single photon timing resolution can only be achieved with small SiPMs because of the large capacitance (100 pF/mm^2) and the SPAD to SPAD time walk. The solution is to use electronics for each SPAD. Monolithic solutions (SPAD and electronics within the same chip) have been developed but impose a trade-off between photon detection efficiency and electronic readout capabilities. This LOI introduces the Photon to Digital Converter (PDC) concept shown in Figure 1 that relies on 3D vertical integration to combine a SPAD array and a CMOS readout chip with digital signal processing to overcome this trade-off and to achieve optimum performances.

The PDC development has been originally pursued by the Université de Sherbrooke together with Teledynde-DALSA in Quebec for applications requiring single photon timing resolution better than 100 ps [1, 2] with scintillating detectors such as Positron Emission Tomography and time imaging calorimeters [3, 4]. The scope has expanded in the last 5 years to experiments being designed to search for neutrinoless double beta decay in liquid Xenon (nEXO) [5] and dark matter interactions in liquid Argon (ARGO). Within the next 10 years, PDCs are expected to become available in various flavors, from front side illuminated (FSI) as shown in Figure 1 to back-side illuminated (BSI) as shown on the left hand-side of Figure 2. Both approaches, FSI and BSI, have their respective advantages to address specific experiment requirements. In both cases the current from the avalanche is sensed by an integrated circuit located under the

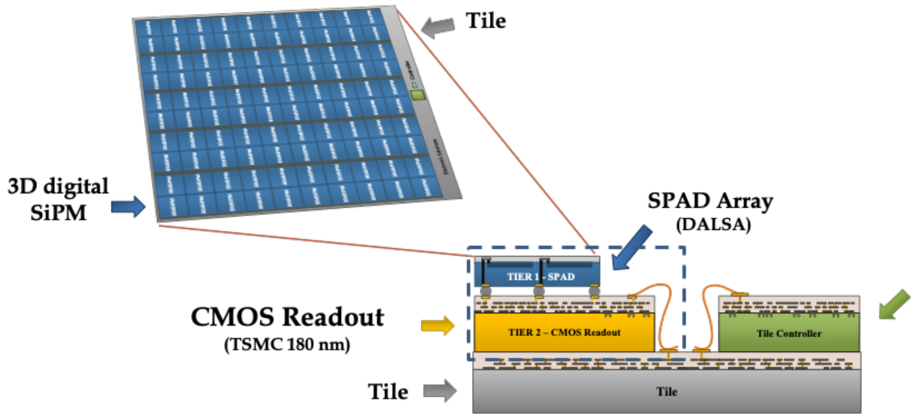

Figure 1: Front side illuminated 3DdSiPM configuration as a 5 by 5 cm^2 tile. The 3DdSiPM itself is the combination of the blue (sensor) and yellow (CMOS) chips. The complete system includes a tile (possibly in silicon) and a tile controller.

SPAD array, as seen in Figure 1. Molecular bonding is expected to be adopted in the future to assemble the sensing and CMOS layers as it has outstanding mechanical stability, reliability and it is becoming an industry standard for 8” to 12” wafers. This technology allows thinning the sensor chip post bonding with the electronics chip. Figure 2 shows three configurations for charged particle detection: 1) keV scale electron detection, 2) minimum ionizing particle detection, and 3) heavy ionizing particle detection. Case 1) shown in the second panel of Figure 2 is being developed within the context of hybrid photo-detector to replace the dynode chain used in vacuum photo-multiplier tube. Case 2) shown in the third panel of Figure 2 is the low gain avalanche diode (LGADs) being developed for application at the high-luminosity LHC and future colliders where timing resolution and radiation damage resistance are critical. Case 3) is mostly applicable to nuclear physics application. Currently the PDC group focuses solely on photon detection, either directly or through the detection of keV electrons. But the PDC concept can be easily expanded to the detection of particles and become the Particle/Photon to Digital Converter (PPDC).

The FSI PDC and PPDC concepts are highly versatile solutions relying on industry standard for 3D integration combined with tailored design for the SPAD array and electronics digital signal processing. We foresee numerous applications in particle physics following the completion of the proof of concept effort that is expected to be completed by 2023. The next phase will be tailoring the FSI PDC and PPDC to their various applications and establishing mass production. In addition, the integration of PDC in complete system will be developed using the latest technologies including silicon interposer, aka silicon printed circuit board and silicon photonics system for data communication.

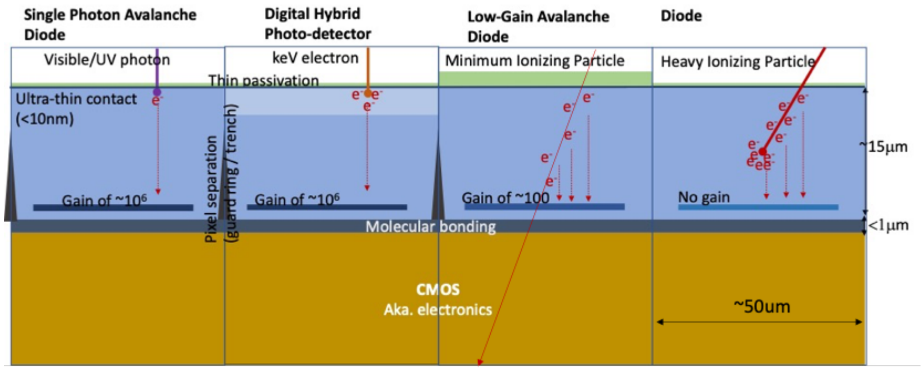

Figure 2: The various flavors of PPDC in the backside configuration showing from left to right the detection of photons, keV electrons, MIPs and heavy ionizing particles.

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