# 3D Integration of Sensors and Electronics
# Snowmass 2020 Letter of Interest

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## 1 Introduction

Three dimensional integrated circuits (3DIC) consist of a suite of technologies which enable bonding and interconnection of multiple layers of electronics and sensors [1]. 3DICs have been widely adopted in cell phone cameras and memory stacks and are a basis for emerging 2.5D and chiplet processes. Technologies developed for 3DICs such as wafer bonding, hybrid bonding, substrate engineering, and multi-tier integration with through-silicon-vias (TSVs) can be combined with innovations from HEP such as Low Gain Avalanche Diodes (LGADs) and 3D *detector* technology to achieve uniquely powerful electronics/sensor assemblies. In this LOI we discuss some examples of applications for these combined technologies which can be studied in more detail as part of the Instrumentation Frontier.

## 2 3DIC SIPM

The Silicon Photomultiplier (SIPM) has become a staple phtotodetector for high energy physics, replacing the photomultiplier in many applications. Although inherently a digital device, the current generation of SIPMs rely on analog summing of the micropixels and resistive quenching of the avalanche. A 3DIC version of the SIPM can incorporate much more sophisticated processing including active quenching for each pixel, digital timing and windowing, intermicropixel communication and digital pattern recognition and readout. Such a device can be tailored to the application and can be more selective and much more powerful that the usual analog SIPM. Prototypes are under development by the Pratte group at Sherbrooke University [2].

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## 3 Edgeless Tile Arrays

Silicon based sensors can be wafer scale, such as the 8" sensors for the CMS High Granularity Calorimeter but electronic integrated circuits are generally limited by the size of the photomask reticule, typically $2 \times 3$ cm or less. This mismatch forces us to engineer complex multi-chip modules where the geometry and functionality of the pixel array is limited by the availability and routing of the external interconnects. The combination of 3D electronics, which provides dense interconnects and vertical through-silicon readout, with active edge sensors that limit dead regions normally associated with silicon detectors, allow us to build fully active tiles. Tiles would be assembled into an array only after they have been fully tested. The only external interconnect are the backside readout bump bonds that are bonded to the detector motherboard. Tiles can populate complex shapes with near-optimal tiling and low dead area. All fabrication processes are wafer-scale, which lowers the processing costs. An active edge sensor array with dummy readout has been fabricated to demonstrate the concept.

## 4 Small Pixel Induced Current Detectors

3D integration allows for small pixels with minimal capacitance associated with the interconnect and electronic processing in complex, multi-tier readout integrated circuits. The resulting signal/noise can exceed that provided by LGADs, which typically have much higher load capacitance. The induced current pulse is prompt, with very fast rise time, and, combined with low capacitance, has the potential to provide excellent time resolution [5]. A fast transimpedance amplifier coupled to the small pixel should provide both excellent time and spatial resolution. In addition to the time resolution provided by the central pixel the detector can also utilize the transient currents determined by weighting field coupling to nearby pixels. Shapes of these output signals depend on the geometry of charge motion within the silicon with respect to the electrode location. The signals shapes can be used to provide track angle information and remove off-angle background tracks. The design of such a device can be flexible, a thin detector to optimize radiation hardness, or a thicker detector to provide information on track angle or charge deposition pattern.

## 5 Double Sided and Small Pixel LGADs

The basic concept of the double sided LGAD consists of a double-sided silicon detector with a gain layer on the electron-collecting side and an array of small (3D-integrated) electrodes on the hole-collecting (anode) side [3]. We assume that the detector is thick compared to the anode pitch. The electron-collecting cathode will observe a fast rise-time signal due to the avalanche in the nearby gain layer while the anodes can provide information on the depth and location of the charge deposition. This complementary approach allows us to measure timing with coarse segmentation in the cathodes and therefore lower the total power and complexity for the timing layer. The anode signal shapes reflect an initial peak due to the primary ionization and a secondary peak a few nanoseconds later due to holes generated in the gain layer. We can use the anode signals to either measure total collected

charge for position resolution or the current pulse shape to measure the depth of the charge deposition at the pixel position.

## 6 3DIC for high performance Pattern Recognition

High performance pattern recognition capability will become more important in the future. Traditionally, pattern recognition capability has been implemented in either FPGAs or conventional ASIC. Adding a "third" dimension opens up the possibility for new architectures that could significantly enhance pattern recognition capability. The 3DIC based architectures allow massive three dimensional network for data communication with much shorter traces and very low parasitic capacitance, with flexible algorithm cells distributed throughout the network. With this kind of data communication network, pattern recognition become much easier and one could even mimic the detector structure for pattern recognition, such as track finding or particle flow over multiple detector layers using both position information and time of arrival information. The basic algorithm cells could be as simple as Content Address Memory cell for simple matching, or could be as sophisticated as NN cells to form a high performance NN network. One simple example [4] is using 3DIC as a way to implement associative memory structures for fast track finding applications.

## 7 Conclusion

3D electronics and sensor integration provide a variety of technologies that can meet the needs of future particle physics experiments. Combining these capabilities with silicon technologies developed for HEP, such as low gain avalanche diodes and active edge sensors, will allow us to design sophisticated detector systems that can meet the increasing challenges of next generation experiments. Crucial to this development is collaboration with partners in laboratories, universities and industry that can provide cost-effective implementations of 3D technologies. The Snowmass study provides an opportunity to explore the potential of these technologies for next generation experiments.

## 8 References

## References


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