Snowmass 2021 Letter of Interest: 4-Dimensional Trackers

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1 Introduction

Precision Timing information at the level of 10-30ps is a game changer for detectors at future collider experiments. For example, the ability to assign a time stamp with 30ps precision to particle tracks will allow to mitigate the impact of pileup at the High-Luminosity LHC (HL-LHC). With a time spread of the beam spot of approximately 180ps, a track time resolution of 30ps allows for a factor of 6 reduction in pileup.

Both ATLAS and CMS will incorporate dedicated fast-time detector layers for the HL-LHC upgrade [1, 2]. Timing information will be even more important at future high energy, high luminosity hadron colliders with much higher levels of pileup. For example, one of the key challenges at a future 100 TeV p-p hadron collider will be the efficient reconstruction of charged tracks in an environment of unprecedented pileup density. A powerful way to address this challenge is by fully integrating timing with the 3-dimensional spatial information of pixel detectors. An integrated 4-dimensional tracker with track timing resolution at the levels of ∼10ps can drastically reduce the combinatorial challenge of track reconstruction at extremely high pileup densities [3].

While timing information will be critical to mitigate the impact of pileup, it is not the only way in which it will enhance the event reconstruction of future hadron and lepton colliders. Timing information offers completely new handles to detect and trigger on long-lived particles (LLP) [2, 4], expand the reach to search for new phenomena by providing new handles on the data [2], and enabling particle-ID capabilities for pion/kaon separation at low transverse momentum [2]. 4D devices with coarse timing capabilities at ∼ns level but with similar granularity as regular tracking devices at the other end of 4D phase space can complement the fast timing layers for an enhanced overall 4D tracking.

2 Towards 4D tracking detectors

The optimal design of future 4D trackers will involve three key considerations: sensors with adequate spatial and time resolution, low power and low noise readout electronics, and overall detector layout, including material considerations. Much work is needed to understand how to best design 4D trackers and to understand the impact of all these aspects on physics performance.

2.1 Sensors

During the last decade, there has been spectacular advances in the development of radiation hard silicon sensors that already today achieve resolutions of approximately 20ps. Examples include Low Gain Avalanche Diodes (LGAD) [5], 3D silicon detectors [6, 7], AC coupled LGDAs [8]. 3D and AC LGAD silicon sensors, in particular, are promising technologies to fabricate small pitch, high precision timing 4D pixel detectors.

For 4D tracking devices with fine spatial resolution and coarse timing capabilities, the monolithic CMOS device ALPIDE deployed in the ALICE Inner Tracker upgrade [9], with $28\mu m$ pixels, is a good reference for state of art fine resolution spatial tracking device. The integration of sensors and readout circuitry on the same die allow the detection of smaller signals and thus thinner devices with fast collection could be produced. The major challenge is the area for the required in pixel circuitry. CMOS MAPS technology used so far are not suitable for deep circuit integration and novel deep submicron technologies need to be explored.

New technologies are making it easier to fabricate thinner sensors and these can generally be applied to planer, LGAD, 3D, or other geometries. For practical reasons, a thin sensitive wafer can be left attached to a thin support wafer at the cost of more material. Use of non-equilibrium annealing methods, allows for the possibility of forming diffusions on the back surface of thinned CMOS MAPS and perhaps of including gain structures with LGAD functionality.

2.2 Electronics

While readout prototypes for the timing detectors at the HL-LHC upgrades have demonstrated performance in line with requirements, applying similar techniques in trackers presents several challenges. High granularity requirement of future trackers will require readout ASICs with smaller pixel sizes compared to present generation, maintaining power consumption levels similar to present designs without timing extraction. Accommodating the additional required electronics for timing extraction, i.e. Time to Digital Converters (TDCs) [10] and memories together with the typical pixel circuitry of present trackers, in pixels at pitches on the order of tens of microns will require the adoption of deeper low power and fast technology nodes beyond 65nm. The entire pixel electronics will need to be designed with low power techniques and with novel timing extraction architecture. In addition, the high luminosity of future hadron colliders will require trackers capable to survive in extreme radiation environments (accumulating a dose of up to 30 GRad and 10^{18} neutrons/cm^2) Because of these aspects, state-of-the-art low power CMOS and Bi-CMOS technology targeted for the mmW communication industry are of particular interest. These includes FDSOI technologies which could potentially open a path to monolithic readouts at very fine pitch. These technologies are also of interest in other HEP applications for their demonstrated performance at deep cryogenic temperatures.

2.3 Layout

A major next step towards 4D tracking at future hadron colliders is the study of how to best combine timing with spatial information. The fine spatial tracking resolution demand towards small pixel with low material budget and low power may make it impractical to instrument finest timing capabilities on all layers. On the other hand, 4D devices with still fine spatial granularity and integrated some coarse timing capabilities can potentially allow a versatile mixture of layers with different balance of spatial and timing resolution to serve an optimal overall 4D tracking for the wide range of applications.

Another aspect of detector layout is related to the physics drivers motivating its development. For example, improved and fast charged track reconstruction, heavy flavor (b/c) tagging, and particle-flow reconstruction under very high pileup density will require 4D information in the inner layers, whereas LLP and time-of-flight particle ID capabilities, including the possibility of strange-tagging [11–14], will benefit from 4D information in the outer layers. LLP applications would demand continuous timing coverage and could benefit from modest timing resolution in more layers without stretching timing dynamic range. Future e^+e^- collider vertex detector backgrounds are predominantly back-scattered bremsstrahlung particles from downstream magnets and collimators with $\sim$ns range delays. 4D tracking devices with fine spatial resolution and modest timing resolution in other layers could significantly enhance the overall performance.

Other key considerations are tracking material and pseudorapidity coverage. The additional material required to go from 3D to 4D tracking will have an impact on the track-time association efficiency and mis-association rate. Whereas a lower track-time efficiency will simply reduce the potential gains from timing information, the wrong assignment of times to tracks is particularly problematic as in this case the 4D reconstruction will perform worse than 3D. The impact of showering of particles within the tracking material might be partially mitigated with the use of advanced algorithms based on graph neural networks or other deep learning techniques but this will require a long term study.

3 Summary

4D Tracking is an ambitious goal for the next generation of particle colliders with the potential of enhancing the power of the experiments to discover new physics and perform precision measurements. Significant R&D on sensors, electronics, and detector layout optimization over the next years will be critical to realizing this goal. We intent to contribute to various aspects of this long-term program.

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