Snowmass2021 Letter of Interest: 28nm CMOS for 4D Tracker Readout Chips

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1 Introduction and Motivation

The present state-of-the-art in HEP instrumentation Pixel detector readout chip technology is being developed by the RD53 collaboration for the High Luminosity (HL) LHC upgrades of the ATLAS and CMS experiments. It uses 65 nm CMOS technology and the half-size demonstrator chip RD53A [1] has been available since December 2017. Test results of RD53A are very promising and the chip performance even exceeds some of its specifications. Since submission of RD53A the RD53 collaboration has been working on the full-size successor, RD53B, which was submitted in March 2020 and is the pre-production readout chip for the ATLAS ITk Pixel detector [2]. With the submission of the RD53B design (March 2020) it makes sense to start investigating how to advance the state of the art into a next generation of even higher performance readout chips. Much of the RD53B design is in fact based on such exploratory work carried out following the previous generation development cycle, that culminated in the FE-I4 readout chip used to build a new inner layer for the ATLAS detector in 2013. Just as that 2013 inner layer upgrade boosted the physics capabilities of the experiment, there is strong motivation for a future replacement of the HL-LHC detector inner layers (both ATLAS and CMS) around 2030. The RD53B chip is designed to withstand a total ionising dose (TID) of 500 Mrad, which will have been accumulated by that time, half way through the physics program. A replacement of the inner layers is thus anticipated in order to complete the physics program, but a replacement with superior technology would boost the physics program.

A particular feature which could open up track reconstruction to new improvements is the addition of high precision time information to the existing high spacial precision, typically called 4D tracking. For example, it can greatly reduce the combinatorial problem of track reconstruction by choosing only hits with consistent time when forming tracks. Preliminary simulations indicate that this could reduce reconstruction time by more than 30% if included only in the expected replacement of the inner two layers of the ATLAS Pixel detector at the High Luminosity LHC. This is a non negligible amount of processing considering the overall amounts of data processing required during the HL-LHC era and could help with potential bottlenecks in computing needs. This of course also translates to detectors at future hadron colliders, as their needs will be in the the order of the HL-LHC or far beyond that.

This R&D project will lay the groundwork which will enable 4D tracking for future Pixel detectors, such as the replacement of the inner layers ATLAS ITk Pixel detector and beyond. We would target a 50 μm by 50 μm pixel pitch (equivalent to the current generation Pixel detectors) with the addition of 100 ps time resolution. The specific choice of 100 ps is driven by the availability of

Table 1: Summary of performance goal for 28 nm prototype and comparison to current 65 nm chip

Specification	RD53B (65 nm)	28 nm	Comment
Pixel capacitance	<100fF	<100fF	Depends on sensor layout
Min. stable threshold	600 e^-	600 e^-	With sensor capacitance
Min. in-time threshold	1200 e^-	600 e^-	With sensor capacitance
Analog power/pixel	5 μW	**5 μW**	
Hit loss from in-pixel pile-up	<1%	<1%	At nominal hit rate
Radiation dose	500 MRad	**1000 MRad**	delivered at -15° C
Timing precision	12.5 ns	**100 ps**	

existing silicon sensor technology which is radiation tolerant enough for operation at the HL-LHC and that it is the upper boundary at which significant performance gains can still be seen.

In order to improve the performance of a 50 μm by 50 μm pixel compared to the present state of art, given by the 65nm CMOS designs of the RD53 Collaboration, it is necessary to target a smaller feature size. 28nm CMOS is the ideal candidate as preliminary studies indicate that its radiation hardness could be sufficient for the usage in an HL-LHC environment.

2 Design and Test Goals

The first prototype chip will focus on the development of the analog front-end, which consists of a low-power charge sensitive amplifier and discriminator. The target of 100 ps timing resolution is a reasonable goal and could also be tested with existing 3D sensor technology[3]. The primary goal of the prototype would be to investigate if such an analog front-end could operate within the power constraints we require and how much area it would occupy or therefore leave to digital readout logic within the pixel. Table 1 summarises the most important performance requirements.

Additionally the chip should include digital and analog circuitry specialised for the characterisation of the influence of ionising radiation, as one of the most important test goals will be to understand the effects of ionising radiation in 28 nm CMOS. The first irradiation campaign results of 28 nm structures [4][5] indicate a behaviour very different to what has been seen in 65nm [6].

In a second step a low power Time-to-Digital converter has to be developed in order to digitise the timing information. As the timing information will likely require more bandwidth to be read out compared to the 4-bit Time-over-Threshold information used in current Pixel detectors, one would also need to investigate what the requirements on the whole readout path are and design low-mass high-speed drivers, receivers, and services.

References

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