Asynchronous First Level Trigger Systems for Future Collider Experiments

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An asynchronous first level trigger system for future collider experiments is proposed. The challenges of distributing and synchronizing stable, low-jitter, high-frequency clocks over a very large distributed system comprised of thousands of optical links will increase to address the needs of the experiments at future colliders. Moreover, the precision of the timing to be maintained will reach the level of tens of picoseconds, and the number of channels and processing boards will greatly increase with the increasing granularity of the experiments. Rather than maintain a synchronous system for the full data path to reach a first level trigger decision, it is proposed to tag the data with a time marker only at the very front-end of the detector electronics and transmit and process the data subsequently asynchronously as is already done traditionally for the data acquisition and high-level triggers after this first level. Effectively, the event builder infrastructure moves to process data at the full rate from the detectors. Already some portions of the first level trigger systems at the LHC experiments run asynchronously: the optical data links connecting the boards comprising the trigger system, for example, do not run synchronously since the frequency of the data link operation does not always match a multiple of the machine frequency. Additionally, some experiments also have introduced a "time multiplexing" approach to serve a complete set of detector data from a particular beam crossing to an individual board of the first level trigger. This proposal just extends this time-multiplexing concept to a fully asynchronous event builder architecture.

A small-scale prototype of such an asynchronous trigger system for the formation of track from the data of several muon detectors was developed and tested in Ref. [1]. The front-end trigger electronics of three spare cathode-strip chambers (CSCs) of the CMS Endcap Muon system were upgraded to perform pattern recognition and bunch-crossing assignment from the anode data at an 80 MHz frequency. Trigger primitives from up to 3 chambers were transmitted via 10 Gb/s serial links to a newly designed track-finding processor, a PC plug-in card, that could generate the asynchronous trigger acceptance signal with a time marker that is sent back to front-end boards for data read-out.

Additional benefits of an asynchronous system include a blurring of the lines between the first level trigger, which typically runs in fast FPGAs, and the higher levels, which typically run on CPUs and now also GPUs. In some sense, a set of FPGA, GPU, and CPU processors can be used to execute a mix of traditionally very fast algorithms for the initial selection of data and more complex algorithms that typically take more time for the final selection.

[1] A. Madorsky, D. Acosta, and H. Patodia, "An Asynchronous Level-1 Tracking Trigger for Future LHC Detector Upgrades", *2006 IEEE Nuclear Science Symposium Conference Record*, San Diego, CA, 2006, pp. 1415-1419, doi: 10.1109/NSSMIC.2006.354166.