Snowmass2021 - Letter of Interest

Superconducting Detectors for High Energy Physics

Topical Group(s): (check all that apply by copying/pasting ☐/☑)

☐ (IF1) Quantum Sensors
☑ (IF2) Photon Detectors
☐ (IF3) Solid State Detectors and Tracking
☑ (IF4) Trigger and DAQ
☐ (IF5) Micro Pattern Gas Detectors (MPGDs)
☑ (IF6) Calorimetry
☐ (IF7) Electronics/ASICs
☐ (IF8) Noble Elements
☑ (IF9) Cross Cutting and Systems Integration

☑ (NF10) Neutrino detectors

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Large superconducting detector arrays are becoming more capable and offer sensitivity that are orders of magnitude better than current work-horse detectors. For example, cryogenic microcalorimeters have demonstrated energy resolution that is 60x better than silicon CCDs for x-ray imaging spectroscopy. These detectors offer single photon sensitivity with very low dark noise and ability to provide both imaging and spectral discrimination of $E/\Delta E$ of greater than 3000 for 6 keV x-rays [1]. Recently, microcalorimeters with 55,800 pixels have been demonstrated by NASA Goddard Space Flight Center using the MIT Lincoln Laboratory's advanced microfabrication processes for the wiring levels [2].

MIT/LL has recently developed a process that supports up to 10 superconducting Nb metal layers for superconducting electronics [3]. Each Nb metal layer is defined by deep UV (DUV) lithography to achieve submicron line/space resolution. The submicron DUV photolithography requires high planarity of circuit layers because of the small depth of focus in modern photolithography. Therefore, the MLT/LL fabrication process utilizes chemical mechanical polishing (CMP) to ensure all metal layers are deposited on a surface with topography height of less than 40 nm. The planarization also simplifies the addition of multiple metal layers by making the process modular – the process for the eighth metal layer can be the same as the process for the second metal layer. Through use of this process, MIT/LL has integrated over 800,000 Josephson Junctions in a single chip [4]. Fig. 1 shows a cross-section of the fabricated chip. This high level of integration has been achieved for the first time in this technology and demonstrates the high-yield of circuits fabricated in the high-density superconductor electronics process at MIT/LL.

This LOI intends to introduce the community to the processing capability at MIT/LL and examples of how this capability is being utilized to support superconducting detectors. In addition to utilizing the process to make large-format microcalorimeters, it is being used to make more sensitive SQUID amplifiers for bolometers [5], very low-power read-out circuits at cryogenic temperatures, and ultra-fast signal processing for these detectors. This white paper hopes to spark collaboration for new detectors that leverages the advanced processes at MIT/LL for advancing high energy physics.

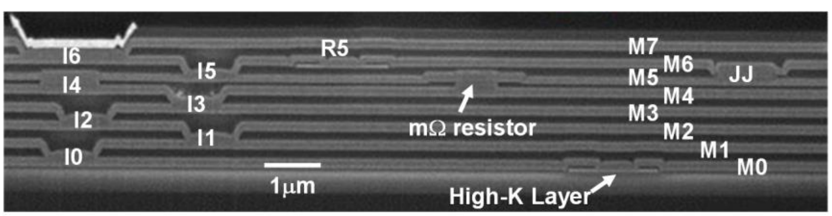

Fig. 1. Cross-section of MIT/LL 8-metal-layer fabrication process with 8 fully-planarized Nb layers marked as M0—M7. Josephson Junction is marked JJ, resistor R5. Etched vias between adjacent layers are marked I0, I1, etc.

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