Snowmass2021 – Letter of Interest

ASICs for Detector Data Transmission

▪ Instrumentation Frontier, IF7: Electronics/ASICs

Jingbo Ye, Dept. of Physics, SMU, Dallas, Texas, 75275. [yejb@smu.edu]

Abstract: In this letter I will discuss ASIC development and R&D work that will double (near term) and quadruple (longer term) the present data transmission rate for particle detectors, enabling a wide range of physics exploration and measurements.

Motivation: The past-decade has seen tremendous advances in particle detector developments, exemplified in pixel sensors [1], high-granularity calorimeters [2] and time (of arrival) detectors [3] for MIPs in a jet. R&D efforts are also seen in dedicated sensor readout ASICs [4], on-detector readout electronics and data transmission to off-detector processing units [5]. In data transmission we have progressed from tens of mega-bits per second (Mbps) per channel to the present 10 Gbps per channel, and migrated from mainly coaxial-cable based transmission medium to optical fibers. At the beginning of the LHC experiments optical link systems were constructed using custom components, COTS (commercial off the shelf) ICs (example: the G-Link chip-set [6]) that are measured to be radiation tolerant, and ASICs developed by CERN (example: the GOL serializer [7]). The transmission speeds range from 80 Mbps to 1.6 Gbps per fiber. With the increase of requirements in data rate and radiation tolerance, and the limit on power dissipation, ASICs become the only choice in constructing the on-detector side of the optical links with a data rate about 5 Gbps [8] per fiber for the Phase-I upgrades of the LHC detectors and 10 Gbps [9] per fiber for the Phase-II upgrades for the HL-LHC. The optical modules also become fully customized [10] for both the Phase-I and Phase-II constructions due to the special requirements on module dimension, channel density, and tolerance to radiation and magnetic field in particle detectors. The electrical-optical signal converters and fibers are identified in the CERN led common project Versatile Link [10] and the focus is now on VCSEL (vertical-cavity surface-emitting laser) and multi-mode fibers that are characterized to be radiation tolerant for applications in the LHC experiments. Given the size of these detectors and the added transmission loss due to radiation a nominal fiber length is chosen to be 150 meters in these R&D projects [11], which matches well with the short-range (SR) fiber optics data transmission in industry, mostly for data centers. This way the R&D in HEP can benefit the advances in industry. Without the requirements of radiation tolerance and very stringent low-power dissipation on components, the data rates in industry for SR fiber links have reached 56 Gbps thanks to fast IC technologies in 28 or even 14 nm CMOS, and transmission schemes such as PAM4 (pulse amplitude modulation with 4 levels). Although in HEP we use COTS, especially FPGA chips for the off-detector electronics, we do not benefit on data bandwidth beyond 10 Gbps because the on-detector transmitter operates up to 10 Gbps. This results in large number of fibers between the on-detector and off-detector electronics (for example the ATLAS LAr readout upgrade will increase the number of fibers from the current some 2,000 to about 40,000) and very low efficiency in the use of the input bandwidth of the off-detector electronics, potentially increasing the number of PCBs and crates there. This limitation may also compromise the detector development preventing its full potential in exploring new physics or providing high precision measurements. For future detectors in HEP, there is a need to increase the channel bandwidth of optical link in the on-detector electronics. The key to this improvement is the data transmitter ASIC.

Proposed R&Ds: CERN through the common project lpGBT [12] has demonstrated 10.24 Gbps transmission speed in the first prototype SerDes (serializer-deserializer) ASIC, also called lpGBT. This ASIC, with its custom transmission protocol and forward error correction capability, is being qualified for applications in the LHC experiments and will be widely used in the upgrades for the HL-LHC or even beyond. CERN is forming working groups to study R&D topics for future experiments [13]. Detector data transmission (WG6) is among the topics and a goal of 56 Gbps per fiber using 28 nm CMOS technology and PAM4 is in discussion. I propose a near term R&D on a low-power and radiation tolerant transmitter with PAM4 all integrated in one ASIC, GBS20, using the TSMC 65 nm CMOS technology. The goal of this R&D is to use two of the lpGBT serializer design blocks with the transmission protocol. The two serializers and the PAM4 encoder will share the PLL also from lpGBT. This will greatly simply the clocking scheme inside GBS20 and eliminate the need of the two CDR (clock-data-recovery) circuits found in commercial PAM4 drivers to save power. GBS20 will re-use lpGBT's C4-BGA packaging option to save the cost of developing the substrate. With this approach, we will have a low-risk and low-cost R&D yet it will deliver an ASIC that will first use PAM4 to double the transmission rate of lpGBT, reaching 20.48 Gbps per fiber. With the same lpGBT transmission protocol, this R&D has the potential of cost saving even on detector constructions in the near future. Just think about the impact of halving 40,000 fibers and reducing the boards and crates accordingly in off-detector electronics. In view of advancing the technology

this will be the first time to design a radiation tolerant PAM4 circuit with VCSEL driver for HEP experiments. Although will not directly participate in this R&D, key designers of lpGBT have expressed support of this project and allowed for the re-use of design blocks from lpGBT. Experience gained in this R&D will enable the SMU group to join CERN future RD projects for higher data rates, up to 56 Gbps, using 28 nm CMOS technology and PAM4. This is the longer-term goal: support the SMU group to work in CERN RD projects on data transmission for future detectors.

Prior work: The final design of GBS20 will be a die of the same size of lpGBT which is above 20 mm^2. This is too large (hence too expensive) for early prototypes. Because of this, we submitted the first prototype GBS20v0 with only the core circuits inside. Without data input, we managed to fit all the circuits into a die of 2 mm^2. The second prototype GBS20v1 will be 4 mm^2, still much smaller than lpGBT. It will have 16 user data inputs each at 1.28 Gbps to fit into the available number of pads without going to a C4-BGA pad arrangement. This is a balance between usefulness of this prototype and the overall development cost.

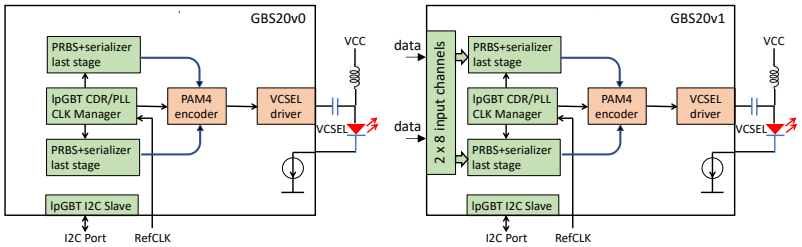

Figure 1. The block diagrams of GBS20.v0 and GBS20.v1

GBS20.v0 is fabricated in TSMC 65 nm CMOS technology and tested up to 20 Gbps, as shown in Fig. 2. The power supply is chosen to be 1.2 V and this is found to limit the dynamic range of the PAM4 driver. When we set a fixed 2:1 ratio of the MSB and LSB inputs to the encoder, we observe significant nonlinearity in the MSB amplitude, which is partially due to the layout. The CTLE technique used to boost the output bandwidth further cuts into the dynamic range of the MSB amplifier. Taken the lessons from GBS20.v0, we are working on the next prototype GBS20.v1, with the following changes: the PAM4 stage operates under 2.5 V to increase the modulation current and leave more headroom for CTLE bandwidth extension. The gain of the MSB and LSB amplifiers is independently controlled to account for nonlinearities not only in the ASIC but also in VCSEL when GBS20 is implemented in a transmitter module. The passive inductance peaking is enhanced. A programmable source load is added to remove the potential peaking overshoot. These design changes allow for an increase of the maximum output current from 10 to 18 mA, maximizing the laser's dynamic range. We plan to submit this prototype in November 2020. As of now the work is supported by SMU internal funds in collaboration with other ATLAS members. I have been seeking for R&D support through DOE's funding opportunity in HEP. Without further support, the current R&D will stop at GBS20.v1.

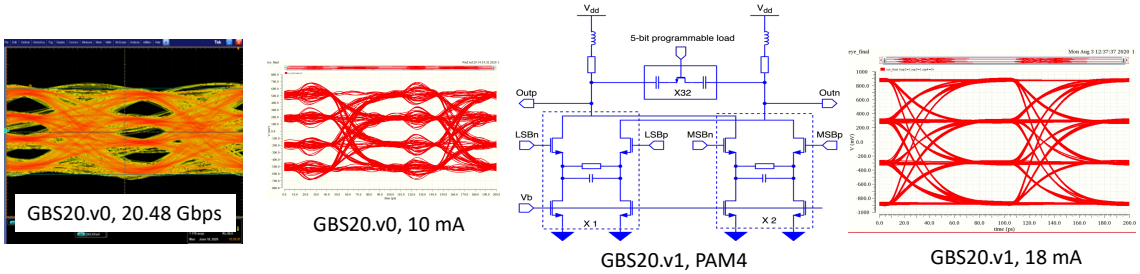

Figure 2. From left to right: the PAM4 output of GBS20.v0 which suffers from bandwidth limitation and the ring from over-peaking; the simulation where the ring is present even with an ideal transmission line; the diagram of PAM4 in GBS20.v1 and the simulated output with the ring eliminated.

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