Quality Control of Cold Electronics Components using Non-Destructive Evaluation Techniques

F. Krennrich[1] (krennrich@iastate.edu), L. Bond,[2] A.J. Weinstein[1], N. Poonthottathil[1]

[1]Department of Physics and Astronomy, Iowa State University, Ames, IA, 50011

[2]Department of Aerospace Engineering, Iowa State University, Ames, IA, 50011

The DUNE Cold Electronics system is the largest implementation of modern ASICs technology in a cryogenic environment [1]. Previous experience with the Fermi-LAT gamma-ray space telescope, the ATLAS hadronic calorimeter and extensive pioneering work done by the Brookhaven National Laboratory group [2, 3] provides a strong foundation for setting the operational parameters to assure a long lifetime for CMOS-based electronics [4]. However, the large scale of DUNE combined with the rapid development and the small physical scale of CMOS technology (now 50 - 200 nm), carry risks during the production of the Cold Electronics system and therefore requires a highly effective QA/QC (Quality Assurance/Control) process. A good understanding of anomalies in the packaging which can potentially affect chip performance and long-term reliability are a key to the success of DUNE.

The main risk for the Cold Electronics system lies in the fact that it has to function reliably for well over two decades inside a cryostat without any access to perform repair and/or replace components. Additional risks come from the multiple cooling and warm-up cycles as is required during the evaluation of the functional performance of the electronics at various stages of integration. Also relevant is the fact that during the testing of ASICs for ProtoDune a low yield of fully functional ASICs and some unexpected deficiencies such as "stuck codes" in ADC-ASICs and "ledge effects" in FE-ASICs were found. While some of the reasons for these deficiencies may have been identified, a good understanding of all of these is essential for establishing a robust QC process. This provides the motivation to search for structural anomalies inside ASICs . For example, stresses in the packing of

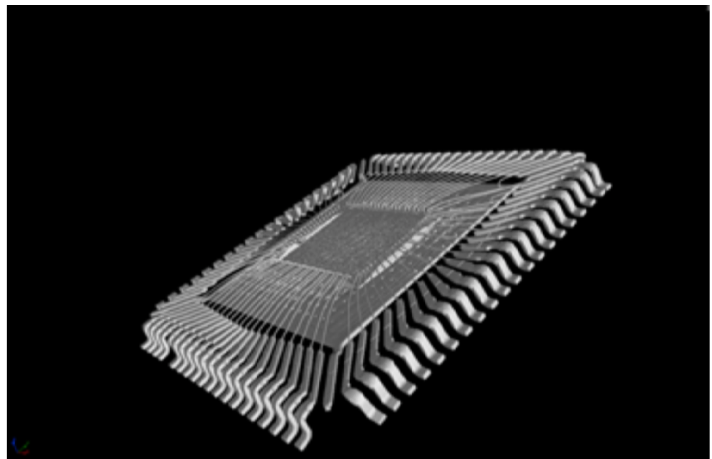

Fig. 1.— - The X-ray micrograph image of a ProtoDune ADC-ASIC using X-ray tomography is shown. The internal structure including wire-bonds and the central circuitry is visible with a spatial resolution of 10 micron.

ASICs could result in stitch-cracking of wire-bonds [5] and/or could change the electronic properties of the sub-micron scale circuit components. A key signature of thermal stresses causing structural changes inside the chip, is anomalies with potential to form de-lamination, a physical separation of layers of different materials or broken wire-bonds.

These considerations provide the motivation to search for anomalies inside the chips' multi-layer structure using instrumentation available to us by the Center for Non-Destructive Evaluation at Iowa State University. Our initial focus was on studies of structural changes inside ASICs as they arise from thermal cycling between room and cryogenic temperatures (88 K).

Our work focuses on two NDE techniques; X-ray computed tomography and scanning acoustic microscopy. X-rays are useful to image high density regions including wire-bonds and printed circuitry at scales down to a micron. X-ray tomography allows one to effectively generate 3-dimensional views of ASICs or printed circuit boards. A projection of a ProtoDune ADC-ASIC is shown in Figure 1. of this section. The wire-bonds that connect the circuitry to the outer pins of the chip are prominently visible. These initial tests confirm that X-ray tomography is a highly sensitive technique to search for defects or stress-induced cracks in the wire-bonds of ASICs and could be used for spot checking of different production runs of ASICs.

Reliability and performance of ASICs may also be affected by thermal stress in the packaging due to manufacturing-related anomalies that can generate defects and could lead to a low yield of functioning chips after multiple stages of cryo-cycling. A sensitive technique for the detection of changes in the packaging of ASICs is given by the Scanning Acoustic Microscopy (SAM) [6]. SAM uses a transducer to generate focused, periodic sound waves onto a small region of a sample, building a complete picture of the sample by scanning this focused beam across the entire surface. Different materials along the path of the sound wave present changes in acoustic impedance, which reveal themselves in phase (timing) and amplitude changes in the reflected wave. The technique is sensitive to both physical structures and structural defects at different depths. SAM is particularly sensitive to structural changes such as *delamination*, a void/gap arising from physical separation between layers of different materials.

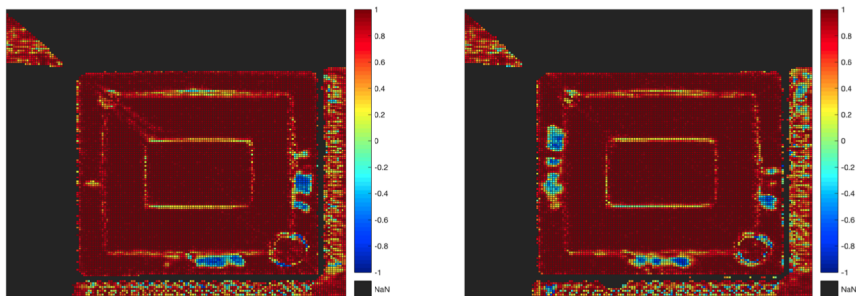

Fig. 2.— The acoustic microscopy (C-scan) images of two ASICs formed using a novel correlation analysis comparing the ASICs before and after treated with liquid nitrogen. A clear change is observed in the sample exhibiting several anomalous features. We have noticed these changes in a few of the samples. The two images correspond to a particular depth inside the sample.

We developed an analysis technique [7] for SAM that allows one to map and compare the internal structure of ASIC chips to each other, using the timing traces that are associated with the reflected waves at the different layers inside the chips. This analysis measures the correlation between timing traces from two different measurements of an ASIC at a given position and allows one to probe for differences at a given depth inside the chip, by simply selecting a specific time window in the timing traces. The correlation analysis has allowed us to compare ASICs from different batches with each other. Furthermore we have carried out studies to follow structural changes for individual chips as they occurred after different stages of cryocycling.

We have seen clearly detectable anomalies in a substantial number of ASICs, as can be seen in these samples (Figure 2). Systematic uncertainties from the measurement setup and the scanning apparatus were determined by scanning the same ASIC chip multiple times showing a systematic uncertainty at the level of 5 percent or less, much smaller than the differences seen in Figure 2.

We are currently in the process of developing a SAM apparatus to perform measurements at liquid nitrogen temperatures to evaluate the structural changes inside ASICs at their typical operating conditions. This technique will be used to further investigate potential changes in ASICs to be operated in liquid argon and get data correlated with both electronic test data and selective destructive/micrographic examination of features seen in images.

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