Snowmass 2021 Letter of Interest: CMOS Deep Cryogenic Electronics for QIS and HEP

Carl Grace (crgrace@lbl.gov), Anastasiia Butko, Maurice Garcia-Sciveres, Timon Heim, Yuan Mei, Aikaterini Papadopoulou, Aritoki Suzuki
Lawrence Berkeley National Laboratory
Mani Tripathi, Jyothisraj Johnson
University of California, Davis
Grzegorz Deptuch, Gabriella Carini
Brookhaven National Laboratory
John Cressler
Georgia Institute of Technology

Thematic Areas: IF7: Electronics/ASICs
IF1: Quantum Sensors

Operation in a cryogenic environment is essential for many quantum sensors and quantum information systems to function [1]. Several HEP applications share this requirement and have been pushing the use of CMOS electronics to colder temperatures, with 70K designs in HEP now widespread (see, for example, [2]). Integrated circuit design in general has been a key HEP technology for many years [3]. However, design of CMOS or BiCMOS electronics for deep cryogenic temperatures, reaching sub-Kelvin, is a new, rapidly growing interest regime for HEP. Cryogenic detectors, operated at cryogenic conditions as low as ~100 mK, are the technology of choice for detection of signals in the electromagnetic spectrum from far infrared through millimeter wavelength, to X-rays, and gamma-rays. Large format, high QE, low-noise detector technologies based on semiconductors provide good performance only in the wavelengths from near UV through optical to near infrared and X-rays. The latter were backed by large both consumer and military investments. For the cryogenic sensors, significant improvement on readout schemes can be made.

The current state of the art readout of superconducting qubits, Transition Edge Sensors (TES), Kinetic Inductance Devices (KIDs), Superconducting Nanowire Single Photon Detectors (SNSPDs), NTD bolometers, etc., uses external electronic equipment seating at higher temperature, from few Kelvins to room temperature. This requires the use of long cables and multiple feedthrough stages resulting in signal attenuation and noise pick up. This adds up to and makes it impossible to match noise levels to those expected if connection from room temperature all the way to sub-Kelvin were only for sending off amplified signals. Amplification, provided by Superconducting Quantum Interference Devices (SQUIDs), high-electron-mobility transistor (HEMT), or parametric amplifiers could be achieved at the lowest temperature so far to provide gain from sub-Kelvin all the way up to room temperature [4]. This approach does not scale well to large channel count, imaging segmentation and disallows compact device geometry.

Operating CMOS technology at temperatures down to 4K and below has been limited by the carrier freezeout in the semiconductor bulk. However, efforts to scale CMOS devices to increase speed and packing density have also reduced the minimum temperature of operation (primarily by increasing electric fields in the channel). Similarly, it has been known that Si bipolar transistors stop working at temperatures as high as 100K, but SiGe heterogeneous bipolar transistors have pushed the operational barrier to sub-Kelvin, offering no threshold voltage increase and a GHz bandwidth at microamperes collector bias currents as additional benefit. The

foundation for understanding performance, power consumption, and reliability of scaled CMOS devices at 4K was done already in the 80's, whereas more recently developing suitable design techniques and simulation models has been carried out at several place, for example at the EPFL Advanced QUantum Architecture (AQUA) Lab and Delft University [5], anticipating the scaling and integration needs of superconducting qubit based quantum computers. Regarding the SiGe technology, pioneering groundbreaking work has been done at the Georgia Institute of Technology [6] demonstrating feasibility of low-noise amplifiers at sub-Kelvin temperatures using SiGe HBTs.

In this proposal we will explore university collaborations to focus on dual use of the developments for QIS and future HEP cryogenic instruments. Regarding process nodes, HEP expertise we will be exploring available CMOS - or BiCMOS nodes from 180nm down to 28nm with widespread access, selecting the best promising one at appropriate costs for small scale HEP prototyping,

The long-term vision of this proposal is to develop deep cryogenic readout chains with digital output, as this will greatly simplify future system development. The key challenges of designing CMOS/BiCMOS circuits at cryogenic temperatures are the lack of adequate device modeling and the requirement for low power circuits, as power is extremely limited by the diminishing cooling capabilities provided by even the best systems at temperature particularly reaching sub-Kelvin levels. The focus of this work will be process characterization, development of circuit networks of low-noise amplifiers, RF control, and readout of quantum systems. The aforementioned challenges will be addressed in two steps. First, various test devices which have already been implemented so far in CMOS or BiCMOS test chips and existing test facilities will be leveraged for characterization and modeling, which will enable successful implementation of cold ASICs [7]. The attention will be given to the technologies and techniques of extremely low power supply levels even below 100mV for achieving ultimate power consumption decrease. The deliverable targeted as the next step will be a low-noise, high-gain amplifier ASIC suitable for example to replace/follow SQUID amplifiers to read out TES sensors. The amplifier will require high sensitivity and extremely low power dissipation. Variants of amplifier circuits, such as a voltage amplifier with high input impedance, and Transimpedance Amplifier (TIA) with low input impedance will be explored. Similarly, high Q-factor RF circuits for resonant control and readout of quantum systems will be proposed and developed. Successful development of these ASICs will pave the way for future work towards cold readout and control ASIC for operation deep cryogenic condition, i.e. at temperature of 4K and below.

References:

[1] Patra, B., et al., "Cryo-CMOS Circuits and Systems for Quantum Computing Applications," *IEEE J. Solid-State Circuits*, vol. 53, no. 1, pp. 309-320, Jan. 2018S

[2] De Geronimo, et al., "Front-End ASIC for a Liquid Argon TPC", *IEEE Trans. Nucl. Sci.*, vol. 58, no. 3, pp. 1376 - 1385, April 2011

[3] Snoeys, et al., "Integrated Circuits for Particle Physics Experiments", *IEEE J. Solid-State Circuits, 35. 184-185, 455*

[4] Dobbs, et al., "Frequency Multiplexed Superconducting Quantum Interference Device Readout of Large Bolometer Arrays for Cosmic Microwave Background Measurements", Rev. Sci. Instrum., 83 073113 (2012)

[5] Charbon, et al., "Cryo-CMOS for Quantum Computing", Proceedings of the IEEE Electron Devices Meeting, 2016, pp. 343-346

[6] H. Ying et al., "Operation of SiGe HBTs Down to 70 mK," in IEEE Electron Device Letters, vol. 38, no. 1, pp. 12-15, Jan. 2017

[6] Beckers, et al., "Cryogenic MOS Transistor Model," IEEE Transactions on Electron Devices, vol. 65, no. 9, pp. 3617 - 3625, Sept. 2018