Snowmass 2021 Letter of Interest: Monolithic Active Pixel Sensors for High Performance Tracking

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Monolithic Active Pixel Sensors (MAPS) detectors have been postulated for charged particle tracking in the early 2000s [1] stimulated by a growing interest at that time in developing lepton colliders with an aim on the International Linear Collider (ILC). The MAPS detectors can be built rather inexpensively, even in large sizes of megapixel arrays, thinned as needed, offer high blooming threshold, individual pixel readout, radiation hardness, while operating at high speed with low power consumption, from a single and low voltage supply. Older-generation MAPS, such as those postulated early for the ILC and practically used in the Heavy Flavor Tracker (HFT) at STAR [2] are built on a low-resistivity substrate, forming the active sensitive volume (ASV) and in-situ signal/data processing is limited. This limitation results from the technological restriction of fabrication processes used for these early MAPS detectors. Simply, a lack of nested n-inside-p doping wells disallows complementary transistors in in-pixel processing circuit networks. Therefore, these early MAPS detectors, although able to offer high granularity and small material budget, are not suited for implementation of the systems requiring advanced timing, fast readout and resistance to radiation needed in the LHC experiments or for Electron Ion Collider.

New inner trackers in Nuclear Physics (NP), such as the Inner Tracker System (ITS1/2) for ALICE on the LHC, managed shifting the MAPS technology, working with the one of the leading image sensor foundry, i.e. TowerJazz (TJ), to the increased resistivity of the active sensitive volume (ASV) and introduction of additional doping steps to form nested wells, etc.. As the results of that, the TJ 180 nm process technology became available to the MAPS detectors designers that allowed significantly to overcome the problem of the early MAPS. In this process, implantations and distributions of resulting electric fields were optimized [3, 4], making possible depletion of ASV and the use of both transistor types for in-pixel circuit networks. Recently, with the advent of the development of the ALICE tracking system upgrade to ITS3 [5], efforts have been made to port the features of the enhanced TJ 180 nm process to the 65 nm node. The new process is becoming available for the developers of a new generation of MAPS detectors. The TJ 65 nm process allows more than four-fold increase of the number of transistors per pixel compared to the older 180 nm. The key benefit of MAPS detectors to be developed in the TJ 65 nm, will be higher spatial resolution and embedment of processing, such as clustering, time-of-arrival or possibly even amplitude measurements in pixels. The development of new MAPS is a synergetic opportunity that has opened thanks to the development of ITS3 for ALICE, and its requirements share high-degree of commonalities with the High-Performance Tracking (HPT) at the EIC at BNL. It is worth noting that features enabled by CERN collaborating with TJ, and offered on the TJ 65 nm, have not been made available working with other vendors so far, whereas an access to the TJ 65 nm process design kits as well as to the previous TJ 180 and is becoming available through CERN.

We envision the described development of the next generations of MAPS sensors proceeding along two parallel paths. The first path is already underway and involves the forming of a consortium of national laboratories and universities to join the CERN ITS3 effort as a path to a next generation sensor for use in EIC tracking[6]. The design goals for the ITS3 and the requirements for an EIC sensor are very well aligned and we expect that, while the design for a specific EIC sensor will need to be forked off from the ITS3 sensor, the commonality in the designs will be very high. CERN welcomes collaborators in this effort and expects that the base designs will be modified by end users who may have differing requirements for their application. The process of participating in this design effort for EIC will familiarize us with the TJ 65 nm process and it's characteristics and capabilities.. This will set the stage for the design work on the applications that extend beyond the use of this process for the EIC sensors, which will comprise the second path.

By this Letter of Intent we postulate harnessing this emerging opportunity and form as early as possible satisfactorily meaningful efforts around the TJ 65 nm process of developing ultra-granular, ultra low-mass, ultra low-power and capable of providing precision timing tracking detectors based on the MAPS technology for the needs practically across all of the offices of the DOE Office of Science, as the MAPS devices to be develop in the TJ 65 nm will posses long-waited revolutionary features also outside of tracking of the collision product.

The short term goals of the proposal will be bringing the TJ CMOS Image Sensor 65 nm processes with quadruple wells, increased resistivity substrate, i.e. ready to operate depleted thinning, to BNL and LBL and other collaborative institutes in the US. Then, the next steps will focus on building basic MAPS structures and participation in the organized Multi-Layer-Reticle fabrication runs for testing and getting the hand-on familiarity with the TJ process. This phase will allow performing studies of optimum properties of active layer, such as thickness, operating voltage, lateral properties due to electric field, etc., required for measurable signal due to the impinging radiation as a function made available by the options on the process. We would like to contribute to the TJ 65nm users' community through developing elements such as libraries, timing models for standard cells, basic blocks, etc. to enable later integration of parallely developed pixel circuits, such as amplifiers, discriminators, time or analog -to-digital converters. event-driven readout blocks, to build ultimately large area detectors. It will also be desired to develop efficient methods for configuring pixel functionality saving on circuital resources that are critical in the planned pixels with side dimensions of O(10um) in the most inner part of trackers.

The long-term vision of this proposal is to develop full size and full functionality monolithic tracking detectors that can effectively replace hybrid detectors, even where high resistance to radiation is required. Certainly hybrid detectors disallow low material budget, are limited in pixel size by bump bonding technology and are more expensive.

References:

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