Trigger extensions for the Scalable Readout System SRS

Snowmass 2021 Letter of Intent

Hans Muller[1],Hugo Natal da Luz[2],Sorina Popescu[3],Lucian Scharenberg[1],Kondo Gnanvo[4],
Alexandru Rusu[5],Dorothea Pfeiffer[6],Richard Hall-Wilton[7]

SRS Scalable Readout System

SRS is a widely used readout system [1] for high channel count detectors, e.g. MPGDs, with up to several MHz per channel readout rates [2]. It consists of a crate-resident backend and a detector-resident frontend with integrated readouts ASICs. The most recent SRS frontend is based on the VMM3a ASIC [3] which includes zero-suppression and configuration settings for a wide range of detectors. The SRS paradigm splits the backend and frontend into fully functional, independent DAQ slices of minimum 128 channels, allowing to start detector R&D with a single, 128-channel "hybrid" to be read out by a crate-based SRS backend and dedicated online software. The addition of more hybrids is in principle unlimited, requires however addition of SRS hardware. Larger systems require more performant PCs or Server-level technology. SRS comes with professional DAQ and controls software associated with default particle physics data analysis tools (ROOT). Channel hit rates in the 1 MHz range may require fast trigger selections in order to reduce bandwidth or alternatively to enhance the physics content of events.

PBX extensions to SRS

PBX is a short acronym for "Power Box with X for cross-linked trigger FPGAs". Optionally inserted into the frontend HDMI links of SRS, the PBX modules allow for implementation of fast triggers in Spartan-7 FPGAs. Bi-directional, high-bandwidth LVDS cable rings can be connected via the PBX front-panels to generate ring topologies for FPGA algorithms working over larger regions. Apart from the trigger extensions, the PBX is an SRS system module which provides local power to a VMM frontend and which operates in one of 4 possible readout modes. Only the ART (Address in Real Time) mode of the PBX is subject of this LoI.

Trigger generation via PBX in ART mode

In the ART mode, the PBX routes hits from up to 1k VMM channels from 8 SRS-VMM hybrids to a single, PBX-resident FPGA. ART is the 5-bit, charge-over-threshold address of the first VMM channel, and preceded by a flag bit. The latency for single-hit addresses from a 1024 channel region arrives in the FPGA over 5 m HDMI links is less than 80ns. Simple local trigger algorithms can complete in O(100-150ns) with trigger outputs both on the front-panels and at the SRS backend. For trigger regions involving multiple FPGAs, and requiring inter-communication over LVDS links, we assume that interlinked regional triggers complete in significantly less than 1us. The current VMM3a version limits the ART feature to single hits per chip and we strongly advocate that next VMM chip revisions should unblock successive ART addresses for multiple hits per chip. Up to 4(8) PBX modules can be stacked in a new PBX Mini(Euro)crate. For triggering purposes, the VMMs are to be configured in the ATLAS mode as opposed to the SRS-default self-triggered mode. Whilst 2D regional triggers, or 3D topology triggers are particularly interesting for confined particle signatures like directional DM events [4], alpha particles counting, or hierarchical triggers in calorimeters [5], basic timing triggers like veto, coincidence, gate, or busy are available through the front-panel. In order to assist the development of standard trigger algorithms the PBX FPGA is mastered by a 32-bit MCU card with USB port. This subsystem allows for development of laptop-based GUIs like already developed for VTC hybrid tester [6] in order to give users or shifters easy access to trigger functionalities and their parameters.

1- Hans.Muller@cern.ch, Bonn University, Physics Faculty, Germany. 2- Inst. of Experimental and Applied Physics, Czech Technical University Prague. 3-IFIN-HH Institute of Physics and Nuclear Engineering, Magurele- Bucharest, Romania. 4-Univ of Virginia Physics Department, Charlottesville, VA 22904, USA. 5-SRS Technology CH-1217 Meyrin, Switzerland. 6- ESS ERIC and Physics Department, Milano - Bicocca University, 20126 Milano Italy. 7-European Spallation Source (ESS ERIC),P.O. Box 176, SE-22100 Lund, Sweden.

Status of SRS with the VMM frontend

SRS is a very mature readout technology developed since 2009 with resources of the RD51 collaboration and using CERN infrastructure and resources [7]. A large number of RD51 collaborators have contributed to its progress and wide acceptance within the MPGD user community. Following a very successful early period with the analogue APV frontend, newer frontend technologies, like SAMPA, Timepix and in the particular VMM have been interfaced to SRS. Based on the latest VMM3a ASIC version developed by BNL for the ATLAS NSW detector [8], SRS was fully redesigned on all levels for commercial SRS production. Ca. 40% of 120.000 ordered VMM channels for 15 teams have been delivered and reference systems are exploring the possibilities given with SRS-VMM [9]. The new PBX can be optionally get inserted into the SRS frontend links to provide longer distances between backend and frontend with four modes of operation. At the time of writing the PBX module is fully specified from the system level down to the schematics and 3D levels. A first prototype implementation is expected by the end of 2020.

Work plan

This LoI represents a call for competences to implement FPGA-based region trigger functionality with GUI-based user control on the new PBX SRS platform. PBX hardware will very soon become available for developers for implementing trigger features at the level of firmware, software, testing and commissioning with the following work plan:

- establish a full set of uPython procedures to access FPGA resources via I2C, SPI and JTAG
- develop a MAC and/or Windows-based GUI for embedded use of uPython procedures
- implement the basic set of standard PBX triggers (fast-or, veto, coincidence, busy)
- add multi-level trigger definitions for region and topology triggers
- establish a common trigger database for the PBX (binaries and sources)
- provide GUI-level parameterization of triggers
- provide a stand-alone, debug-level test environment without SRS backend
- establish a standard user guide for shifters

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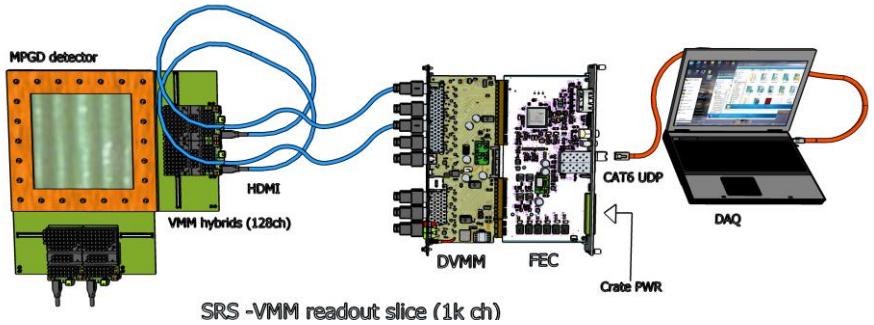
Backup pictures

VMM hybrid



SRS -VMM readout slice (1k ch)