Lincoln Microelectronics Foundry

Letter of Interest, SnowMass 2021

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High capability integrated circuit access is a challenge for academic and scientific communities. Commercial facilities aren't rewarded for small volumes or process customization; non-commercial facilities will customize processes but seldom have process controls and systems to support high layer counts or substantial circuit and detector integration.

Lincoln Microelectronics Foundry has a commercial-class 200mm silicon fab providing custom integrated circuits for national security and science. We operate 3-shifts, five 24-hour days per week with ISO-9001 certification and DoD Trusted Foundry certification since 2015. With well over 100 tools and 500 process control charts, we have broad process capability supporting a number of computing and sensing technologies including

- 90nm fully depleted silicon on insulator (FDSOI) CMOS with extreme environment variants
- Silicon and germanium charge coupled device (CCD) imaging
- Integrated photonics in several waveguide materials
- Superconducting circuits for transition edge sensors, low-energy high-speed digital and quantum computation
- GaN-on-Si circuits for microwave integrated systems
- Heterogeneous integration at the wafer and die level.

We resolve single patterns down to 90nm with our 193nm ASML PAS 5500/1100 scanner over a 23x32mm field with its 0.75NA lens. The scanner is coupled to our TEL ACT12 track system for a full-flow integrated 193nm lithography cell. We scale to pattern larger dimensions with 248nm Canon EX4 stepper (22mm square field) and 365nm Canon iW stepper (50mm square field). We regularly stitch fields within and between lithography platforms to provide large format devices and can direct write them down to 1um resolution across a 200mm wafer utilizing a Heidelberg maskless exposure system, mitigating reticle costs and exposure complexity for very large devices. We also have spray coating for patterning high topography wafers with broadband and i-line resists.

We have processes and systems that yield many-layered circuit fabrication including planarized interconnect metallization and defect management through automated patterned-wafer defect identification. We manage defects through an enterprise database system, populated from our detection tools and providing analytics including step contribution and classification that reveal process integration issues for resolution. We model and control defects for several technologies with these tools to meet monolithic integration challenges; this has special benefit for large format devices.

We welcome multi-project wafer collaboration and have a have done so both in established technologies like CMOS and newer ones like digital superconducting development under iARPA and DARPA sponsorship. We also partner to customize processes for research and development as well as limited delivery programs. Lastly, Lincoln Laboratory has a history of supporting DoE efforts both through Interagency Agreements and through collaboration agreements with DoE performers.

Please contact MEL.Director@ll.mit.edu for collaboration interests.

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