Mu2e-II: a 2-level TDAQ system based on FPGA pre-filtering
Letter of Interest for Snowmass 2021

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The Mu2e experiment at Fermilab will search for a charged lepton flavor violating process where a negative muon converts into an electron in the field of a nucleus. Mu2e-II, a proposed upgrade of Mu2e, aims to improve the expected sensitivity by at least an order of magnitude over Mu2e. In this paper we discuss the conceptual idea for the TDAQ system of Mu2e-II based on 2 levels: a L1 hardware layer (based on FPGA) followed by a High Level Trigger stage.

I. INTRODUCTION

Lepton flavor violation (LFV) has been observed in the neutral sector (neutrino oscillations), but not in the charged sector. In the Standard Model, the predicted rate of charged lepton flavor violating (CLFV) processes is below 10^{-50} [1]. However, many theories beyond the Standard Model predict CLFV processes with rates observable by currently constructed HEP experiments [1]. The Mu2e apparatus includes three superconducting solenoids: (1) the production solenoid, where an 8 GeV proton pulsed-beam (period 1.7 μs) hits a tungsten target, producing mostly pions; (2) the transport solenoid, which serves as a decay "tunnel" for the pions, and makes also charge and momentum selection, creating a low-momentum μ^- beam; (3) the detector solenoid, which houses an aluminum Stopping Target, where the muons get stopped and form muonic atoms, and the detector system (in a 1T solenoidal magnetic field) optimized to detect e^-/e^+ from the conversions. The entire detector solenoid and half of the transport solenoid are covered with a cosmic-ray veto system (CRV), made out of 4-layers of extruded scintillator bars.

Mu2e II, an evolution of the Mu2e experiment, will continue to search for the muon to e^-/e^+ conversion processes with a significantly improved discovery potential over currently planned projects. The anticipated single event sensitivity (SES) of Mu2e is 3×10^{-17} for scattering on an aluminum nucleus. The current best limit is from SINDRUM II on gold, $R_{\mu e} < 7 \times 10^{-13}$ [2].

II. ASSUMPTION AND REQUIREMENTS FOR THE TDAQ SYSTEM

Mu2e-II relies on the existence of a more powerful source of protons, the PIP-II linac [3], under construction at Fermilab. This will provide $\sim 1.4 \times 10^9$ 800 MeV protons/pulse for Mu2e-II, compared with 3.9×10^7 8 GeV protons/pulse at Mu2e, with 1.7 μs pulse spacing. In addition to that, Mu2e-II plans to increase the beam duty cycle by a factor $\times 4$ w.r.t. Mu2e. Due to the higher instantaneous muon rate, anticipated to be larger of a factor of 3 than in Mu2e, and due to the better duty cycle, the foreseen total data rate in Mu2e-II will increase of a factor >10. On the other side, the design of the Mu2e-II experimental setup is not yet finalized and it is still evolving as part of the Snowmass-2021 process. In order to set the requirements for the TDAQ system, we assume that Mu2e-II will adopt a similar experimental setup as Mu2e, but will improve granularity of detector elements up to a factor of 2. The direct consequences of these assumptions are:

- an increase in the event data size by a factor of $\sim \times 6$; $\times 3$ due to the instantaneous rate and $\times 2$ due to the number of channels, reaching a level of 1 MB/event;
- a reduced period when no beam is delivered to the apparatus, which in Mu2e is 1 s out of 1.4 s;
- a factor of $\sim \times 10$ larger dose on the electronics;

Assuming that the Mu2e-II storage capacity on tape will be twice that of Mu2e, reaching $\sim$

14 PB/year (equivalent to a few kHz), the required trigger rejection needs to be a factor of ~ 5 better than in Mu2e (in Mu2e is expected to be at the level of a few hundreds).

III. FROM MU2E TO MU2E-II

Mu2e uses *artdaq*[4] and *art*[5] software as event filtering and processing frameworks respectively. The detector Read Out Controllers (ROC), from the tracker and calorimeter, stream out continuously the data, zero-suppressed, to the Data Transfer Controller units (DTC). The data of a given event is then grouped in a single server using a 10 GBytes switch. Then, the online reconstruction of the events starts and makes a trigger decision. If an event gets triggered, we pull also the data from the CRV and we aggregate them in a single data stream. Figure 1 shows a scheme of the Mu2e data readout topology described above.

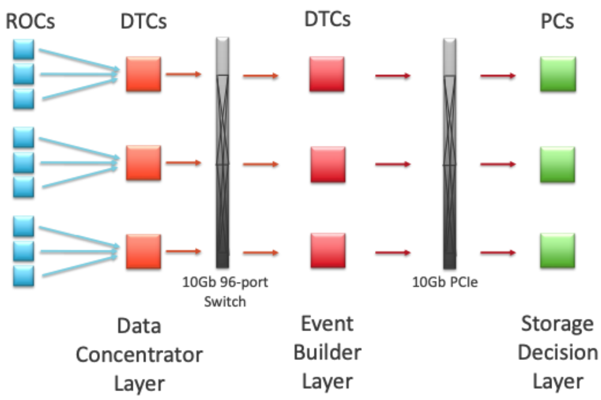

FIG. 1. Mu2e data readout topology.

The Mu2e main physics triggers use the info of the reconstructed tracks to make the final decision. The Mu2e Online track reconstruction is factorized into three main steps [6]: (i) hits preparation, where the digitized signals from the subdetectors are converted into reconstructed hits, (ii) pattern-recognition to identify the group of hits that form helicoidal trajectories, and finally (iii) track fit through the hit wires, which performs a more accurate reconstruction of the track.

For Mu2e-II one of the ideas is to implement a L1 hardware trigger that exploits the first two stages of the Online track reconstruction on a dedicated FPGA based board and then exploit the rest of the reconstruction on the commercial servers. The major challenges are represented by: (a) the amount of data that needs to be concentrated on a single board and (b) the migration of a non negligible part of the Online reconstruction onto an FPGA. For the first one, the system will need to use more performant rad-hard optical transceivers (an R&D is already ongoing at CERN), which are needed to stream the data from the ROCs to the data-concentrator layer, and a more powerful switch (100 Gb switch are already available). For the second one, it's important to realize that FPGA development can take place now – hardware is not needed! Starting now would help the understanding of required resources and in consideration of topology trade offs. For example, what size FPGA is best suited, or what are the advantages and disadvantages of commercially available hardware versus established custom boards in the community versus creating a new custom board. In the last decade, a new tool named High Level Synthesis (HLS) [7] has been developed to rival manual VHDL or Verilog algorithm development. The major HLS features are: (i) it allows non-specialists to easily understand and develop low and fixed latency FPGA algorithms, (ii) it simplifies offline emulation, (iii) it facilitates debug and verify in a software environment (often 10x faster iterations than firmware simulation tools). We also note that other HEP collaborations, like the CMS experiment at CERN, have been heavily investing in HLS approach to FPGA algorithm development. Interestingly, the Mu2e run plan offers the possibility to test (parasitically) a prototype of a L1 trigger board in the second phase (after the LBNF shutdown). Leveraging Mu2e as a live data source would give valuable feedback for advancing Mu2e II's R&D phase.

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